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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/461,643	12/14/1999	KEITH DOW	10559/108001	4089

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EXAMINER
LEE, CHRISTOPHER E

ART UNIT	PAPER NUMBER
2189	19

DATE MAILED: 08/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No. 09/461,643	Applicant(s) DOW, KEITH	
	Examiner Christopher E. Lee	Art Unit 2189	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 24 July 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☐ The period for reply expires _____months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☒ The proposed amendment(s) will not be entered because:

(a) ☒ they raise new issues that would require further consideration and/or search (see NOTE below);

(b) ☐ they raise the issue of new matter (see Note below);

(c) ☒ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

(d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: *See Continuation Sheet*.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a)☒ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: *none*.

Claim(s) objected to: *none*.

Claim(s) rejected: *1,3-8,10-14,16-20,23 and 24*.

Claim(s) withdrawn from consideration: *none*.

8. ☐ The proposed drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

Paul R. Myers

PAUL R. MYERS
PRIMARY EXAMINER

Continuation of 2. NOTE: The amendment filed on 24th of July, 2003 under 37 CFR 1.116 in reply to the final rejection has been considered but is not deemed to place the application in condition for allowance and will not be entered because the proposed amendment raises new issue that would require further consideration and/or search, which is "where said first layer defines a non-grounded gap between said first and second portions of the first and second lines" in the claim 1, as an exemplary amended claim. Even though the Applicant asserts all of the elements and their relationships claimed in the amended claims were either earlier claimed or inherent in the claims as examined, the amended claims would require further consideration and/or search because the amended claims extend the scope of the claimed invention and/or were not previously addressed in the Final Rejection.

Continuation of 5. does NOT place the application in condition for allowance because: In response to the Applicants' arguments regarding to the prior art rejection, the arguments are drawn to limitations which have not been entered for consideration .

In response to the Applicant's argument with respect to "First, the parallel signal lines shown throughout Perino are connected to different pins on two connectors, rather than to a single first pin as in claims 1 and 20. ... Perino thus fails to describe or suggest first and second signal lines both connected to a first pin on a memory unit and having substantially parallel second portions, as per claims 1 and 20" on the Response page 11, lines 7-19, the Examiner respectfully disagrees. In contrary to the Applicant's statement, AAPA teaches said first and second signal lines both connected to a first pin on a memory unit, and Perino teaches a portion of a signal line is substantially parallel to a portion of another signal line (See the Paragraph 6, claim 1 rejection in the Final Office Action mailed on 28th of May, 2003). Then, the Examiner has clearly pointed out rationale for appropriate combination of the references AAPA and Perino. Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicant's argument with respect to "Secondly, Perino explicitly teaches away from separating second portions of signal lines by a non-grounded gap. ..." on the Response page 11, line 20 through page 12, line 4, the Applicant argues with the amended claim's issue' such that 'separating second portions of signal lines by a non-grounded gap', which needs further consideration because the amended claim extends the scope of the claimed invention. Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicant's argument with respect to "Finally, the impedance mismatch referred to in page 4-5 on the Office action arises due to the high impedance of signal lines that are relatively narrow to accommodate 'two-between' routing ... Thus, according to Perino, the teachings relied upon in rejecting claims 1 and 20 are disadvantageous. ..." on the Response page 12, lines 5-16, the Examiner believes that the Applicant misinterprets the claim rejection. The Applicant essentially argues that Perino teachings relied upon in rejecting claims 1 and 20 are disadvantageous. Perino discloses the impedance mismatch causes reflected signals, thus degrading signal integrity and limiting operating frequency (See Perino, col. 2, lines 25-29). However, in contrary to the Applicant's statement, the Examiner has clearly pointed out rationale for appropriate combination of the references AAPA and Perino, such that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have motivated to employ the concept of the line width and space determination, as disclosed by Perino, to said circuit board routing, as disclosed by AAPA, so as to make (1) a second portion of said first signal line and a second portion of said second signal line route with a separating distance, and (2) said signal line widths of said first and second signal lines are equal to the width of said separating distance for the determined impedance values, for the advantage of (1) eliminating reflected signals and signal deterioration caused by a mismatched impedance, and (2) eliminating reflected signals and signal deterioration caused by a mismatched impedance (See Perino, col. 5 lines 29-32). Thus, the Applicants' argument on this point is not persuasive.

In response to applicant's argument that the Examiner's conclusion of obviousness for the 35 USC §103(a) rejection fails to establish a prima facie case of obviousness, the Examiner respectfully disagrees. In contrary to the Applicant's statement, all the rejections under 35 USC §103(a) in the prior Office ActionS established a prima facie case of obviousness meeting the three basic criteria of the M.P.E.P. 2143.03 (8th ed. 2001). Furthermore, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the Examiner has clearly pointed out rationale for appropriate combination of the references. Thus, the Applicants' argument on this point is not persuasive.